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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------|------------------|
| 09/809,639 | 03/15/2001 | Jacob Oshins | 50037.27US01 | 5084 |
| 23552 | 7590 | 02/10/2004 | EXAMINER | |
| MERCHANT & GOULD PC P.O. BOX 2903 MINNEAPOLIS, MN 55402-0903 | | | VO, TIM T | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2112 | |
| DATE MAILED: 02/10/2004 | | | | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|------------------------------|------------------------|---------------------|--|
| | 09/809,639 | OSHINS ET AL. | |
| Examiner | Art Unit | | |
| Tim T. Vo | 2112 | | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 30 December 2003.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-20 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a))

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ .

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____

Part III DETAILED ACTION

Notice to Applicant(s)

This application has been examined. Claims 1-20 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-18 are rejected under 35 U.S.C. § 102(b) as being anticipated by Reneris patent number 5,903,894 referred hereinafter "Reneris".

As for claims 1, 7 and 19-20, Reneris teaches a computer implemented method for accessing data, comprising:

receiving a first request to access data associated with a PCI device (see figures 3A-3B and column 11 line 60 to column 12 line 54 and column 6 lines 15-36, wherein computer system 5 starts at step 305 where the BIOS 17 configuring for PCI devices coupling on the PCI bus 18, the configuration is directed to a system for controlling and identifying controllable hardware devices connections between the devices using a hierarchical data structure (HDS 40). The HDS 40 stores information about the computer system and devices with the computer and is used as a reference by software modules, such as an operating system. Wherein the first request is when the HDS

identified a PCI device on the PCI bus 18), the first request being received at a system for maintaining a namespace containing a plurality of software objects describing hardware devices associated with a computer system (see figures 3A-3B and column 12 lines 42-55 and column 13 lines 5-30, wherein devices are identified by the device object), identify the first request to access the data as being associated with a defined operation region associated with the PCI device (see figures 3A-3B and column 12 lines 9-12), passing the first request to a provider registered to handle access to the PCI device, the process provider comprising a generic driver that is programmed to resolve and maintain addressing information for a plurality of PCI devices, including the PCI device (see abstract and figure 8 step 805, 810, wherein the abstract teaches that the information systems saves to the hierarchical data structure (HDS) during operations such as plug and play (PnP, column 1 lines 23-25). The information saves in the HDS 40 such as data object includes device ID, configuration information, device power states etc., (column 13 lines 5-30) thus, other information saves through various storages (205, 210, 225 etc.), which discloses in figure 2 to serve operating system 36. Further, column 19 lines 23-67, Reneris teaches an operation system 36 (process provider) utilized information saved in HDS 40 and other 205, 210, 225 etc. to load conventional drivers 37 (generic driver) to accommodate identified PCI devices in the system).

As for claims 2-3, Reneris teaches receiving data returned from the provider (see figure 7, step 725); and
passing the returned data to the requesting component (see figure 7 step 735).

As for claims 4 and 11, Reneris teaches wherein the defined operation region comprises a PCI BAR Target operation region of the configuration management system (see column 12 lines 42-55).

As for claim 5, Reneris teaches wherein the first request to access data associated with the PCI device comprises a command generated by firmware associated with the computer system (see column 9 lines 57-65).

As for claims 6 and 9, Reneris teaches wherein the command generated by the firmware comprises a control method request to access the data, the control method being one of the software objects within the namespace (see column 12 lines 50-55).

As for claim 10, Reneris teaches wherein the configuration management system comprises an Advanced Configuration and Power Interface system (see figure 1, ACPI 38).

As for claims 12-13, Reneris teaches wherein the definition block further includes executable instructions for creating a control method that, when executed temporarily use of the operation region and notify the configuration management system of a change in the availability of the operation region (see column 2 lines 29-38).

As for claims 14-18, Reneris teaches base address identifying an address space with which the effective address location resides (see figure 5 and column 15 lines 1-30).

Response to Arguments

2. Applicant's arguments filed 12/30/04 have been fully considered but they are not persuasive.

3. In response to the applicant arguments that Reneris fails to teach a generic driver. Column 19 lines 23-67, Reneris teaches an operating system 36 (process provider) utilized information saved in HDS 40 and other information saved via 205, 210, 225 etc. thus manipulating the information given in order to load conventional drivers 37 (generic driver) to accommodate identified PCI devices in the system).

4. In response to the applicant arguments that Reneris neither teaches nor suggests having a process provider that resolves and maintains addressing information for a plurality of PCI devices. On page 7 of remarks, applicant admitted that Reneris teaches a system is directed at solving the following problems: 1) describing hardware devices to the operating system; 2) describing connections or dependencies between devices; and 3) providing extensible and abstract methods of controlling devices executable by the operating system or any other software module, such as BIOS routines. Further, on page 8 of remarks, applicant admitted that Reneris teaches that the operating system loads an appropriate device driver for each of the identified devices. These evidences, which admitted by the applicant that Reneris utilizes either operating system or BIOS routines to control the PCI devices on the PCI bus 18, thus Reneris teaches "a process provider that resolves and maintains addressing information for a plurality of PCI devices" i.e. operating system (OS 36) or BIOS routines as being "process provider". see explanation below:

5. As described by the examiner in the previous office action, pages 2-3, Reneris teaches firmware BIOS routines for a computer system for configuring PCI devices coupling on the PCI bus 18. Reneris teaches the hierarchical data structure (HDS 40)

for controlling and identifying PCI devices coupling on the PCI bus 18. The HDS 40 identified each PCI device on the bus 18 with information about that particular device such as, ID device, device driver ID and then passes the information to the Operating System (OS 36). The Operating System (OS 36) gathered information given from the HDS 40 such as ID device, device driver ID for each device identified on the PCI bus 18 and utilizes ACPI driver and address given from the Root System Description Table (RSDT) (step 325) to locate the right device driver in order to load appropriate device driver for each PCI device on the bus 18. Further, column 2 lines 8-14, Reneris teaches controlling hardware as described above is also controlled by the BIOS routines (firmware).

6. As described above, Reneris teaches either the operating system (OS 36) or any other software module, such as the BIOS routines (firmware) is being equivalent to the "process provider" of the current invention as claimed as being programmed to resolve and maintain addressing information for a plurality of PCI device.

7. In response to the applicant arguments that Reneris neither teaches nor suggests "a definition block including a PCI object that defines an operation region for accessing a firmware controlled PCI device". As discussed above, Reneris utilizes HDS 40 to identify PCI devices coupling to the PCI bus 18 with information about that particular device such as, ID device, device driver ID and passes to the operating system or accessing the BIOS routines firmware to control the PCI devices.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim T. Vo whose telephone number is 703-308-5862. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tim T. Vo
Primary Examiner
Art Unit 2112

2/7/04